

363	65	Subclass
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ISSUE CLASSIFICATION

PATENT NUMBER

RE38140

RE38140

## U.S. REISSUE Patent Application

O.I.P. # 12W 103 SCANNED G.A.	O.G. PUBLICATION DATE 4-17-2001	REISSUE PATENT DATE JUN 10 2003
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APPLICATION NO. 09/781120	CONT/PRIOR D	CLASS 363✓	SUBCLASS 65	ART UNIT 2838	EXAMINER Berkey
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Gregory Schaffer

PARENT FILE  
OF REISSUE  
APPLICATION  
10/409,538

Dual interleaved DC to DC switching circuits realized in an integrated circuit

PTO-2  
12/9

☒ SURRENDER OF ORIGINAL PATENT EB (Exr. Initials) ORIGINAL PATENT NUMBER 5,810,216

**ISSUING CLASSIFICATION**

ORIGINAL			CROSS REFERENCE(S)			
CLASS	SUBCLASS	CLASS	SUBCLASS (ONE SUBCLASS PER BLOCK)			
365	65					
INTERNATIONAL CLASSIFICATION		323	282			
402M	7/00					

☐ Continued on Issue Slip Inside File Jacket

<input type="checkbox"/> <b>TERMINAL DISCLAIMER</b>	<b>DRAWINGS</b> Sheets Drawn: 4 Figs. Drawn: 5 Print Figs.: 2d		<b>CLAIMS ALLOWED</b> Total Claims: 63 Print Claim for O.G.: 22	
<input type="checkbox"/> The term of this patent subsequent to _____ (date) has been disclaimed.	_____ (Assistant Examiner) (Date)		<b>NOTICE OF ALLOWANCE MAILED</b> 12/12/02	
<input type="checkbox"/> The term of this patent shall not extend beyond the expiration date of U.S. Patent. No. _____	_____ (Primary Examiner)		<b>ISSUE FEE</b> Amount Due: 1280 Date Paid: 12-18-02	
<input type="checkbox"/> The terminal _____ months of this patent have been disclaimed.	_____ (Primary Examiner)		<b>ISSUE BATCH NUMBER</b>	
<b>FINAL SPRE REVIEW</b> _____ (INITIALS)	_____ (Legal Instruments Examiner)		_____ (Date)	

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